Attachment 1

Title: WOLA Filters and Auto-tuning for Radio Astronomy

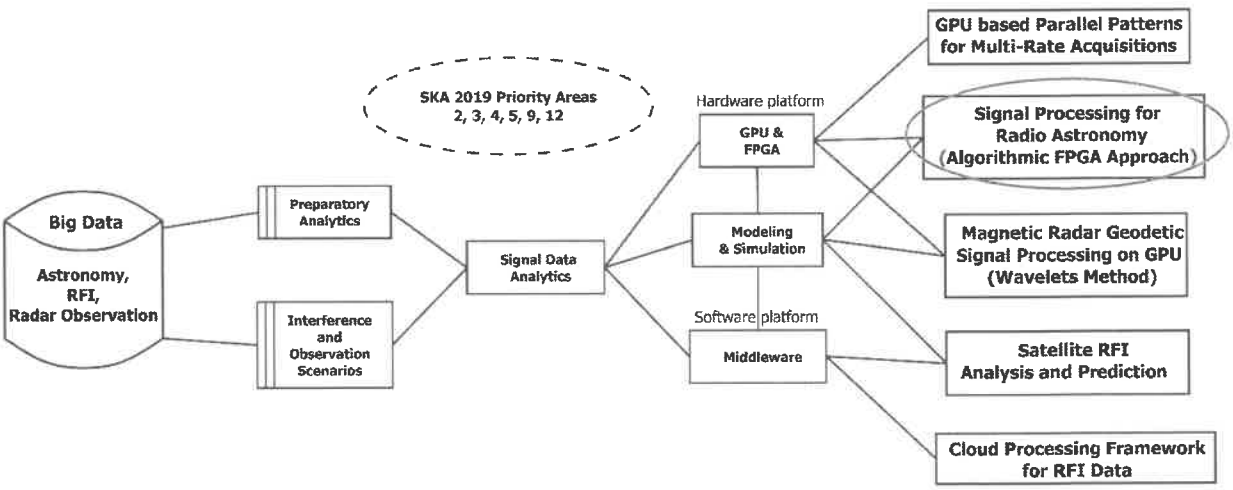
Section A: Overview of the Research Project Proposal

1. **Academic level of research project:** Master's (upgradable to PhD re auto-tuning desires)
2. **Broad field of research:** Engineering
3. **Title of the research project:** WOLA Filters and Auto-tuning for Radio Astronomy
4. **Full names of supervisor and co-supervisor:** Dr Simon Winberg
   (availability of co-supervisor expected)
5. **University where postgraduate student would be registered:** University of Cape Town

Section B: Full Research Project Proposal

Research project abstract:
Propose implementing Weighted OverLap Add (WOLA) filterbanks in hardware (preferably FPGA, alternatively GPU) to, among other things, reduce spectrum leakage during astronomy signal processing, as well as to attempt to boost the performance in relation to amount of logic area used on FPGAs compared to other methods (e.g. the more standard polyphaser folders approach).

This proposal arches to our bigger project view, shown below, in the skill development areas of FPGA/GPU hardware, instrumentation and data analytics that are related to the SKA requirements.



1. **Scientific Merit:** Many digital signal processing computations are based on Discrete Fourier Transform (DFT) which results in spectral leakage. The leakage might contain useful information in the radio astronomy data and would be lost as such. This can be circumvented with a better technique known multi-rate polyphase channelizer; in this project we propose to use WOLA filters, which operate in a similar way to polyphse filters, to provide an even more efficient version for deployment on FPGAs, using the weighted overlap and add technique. This is expected to utilize few logic elements than standard polyphaser implementation, but we need to see if similar benefits can be achieved, particularly reducing spectral leakage.

   In terms of the auto-tuning aspect, we propose following the system that has been applied in the SDRLift tool, a tool that was developed by a previous PhD student in the research group, for which a data flow model is produced, HDL cores connected, and profiling of predicted performance is then performed prior to automatic generation of HDL glue code that integrates

the cores (following pre-defined interfacing specifications). The tool help direct the user to find bottlenecks or areas that may potentially restrict performance. Ideally, this project will be able to take SDRLift further through implementation of WOLA filtering support, possibly by adjusting the coded requirements to support representing points in the design in which a WOLA filter is needed, and then enhacing the profiling methods to account for the behaviour and logic utilization of these filers. These additions will require a thorough understanding of the way WOLA is implemented, consideration of the RLT representation, and performance factors. Accurdingly, taking the project further into this direction of enhancing SDRLift would be recommended as a PhD project.

2. **Feasibility:** Many radio astronomy telescope facilities around the world are switching to polyphase filtering(PFF). A standard PFF is computationally expensive. But the resultant response is flatter and spectral leakage is less. WOLA poses similar advantages but in a form that is computational simpler, and thus expected to be easier to implement on an FPGA. Therefore, we propose a FPGA-based parallel embedded processing solution. The filterbank can also be used in up/down-conversion or up/down sampling typically arising during hetero/homodyning. The technique is useful for spectrometry, RFI or radio astronomy where useful information may be buried in the spread spectrum. The student will be required to develop a cascaded digital filterbank that is sized at elaboration before synthesis according to device resources. Additional requirement is to prove out the filterbank in simulation (before physical synthesis) for acceptable group delay, frequency response, and minimal resolution of coefficients.

3. Link to SARAO priority areas: This project connects to three areas: 2 i.e., signal processing using FPGAs/GPUs.

4. Student profile: BSc/BEng degree in electronics or electrical engineering from ECSA recognized university or equivalent. Background (coursework, thesis /project, internship or job experience) in communication, signal processing and digital radio will be highly useful along with good analytical and problem solving skills.