Section A: Overview of the Research Project

1. Single-package receivers for aperture array radio astronomy
2. Engineering
3. Doctoral

4. The SKA Mid-Frequency Aperture Array (MFAA) will make use of aperture array antennas in the 500 – 1500 MHz range. Each of these antennas would need a low noise, but uncooled receiver. Monolithic or co-packaged integration of such a receiver would allow for low-cost mass-production, but there are several shortcomings to the state-of-the-art that need to be addressed first. The integration of the low-noise amplifier (LNA), the true time delay circuit (TTD) and the analogue-to-digital converter (ADC) poses several significant problems, including the broadband calibration of the time delay, as well as ADC switching noise leaking into the LNA input. There are methods that may be adopted to mitigate these problems (EBG shielding, co-packaging of separate dies, built-in self-calibration), but have not been applied in this context. This PhD study will build on a prior M.Eng study, expanding the scope of research to implement noise mitigation and the self-calibrating TTD circuit.

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Section B: Details of Research Project

1. Scientific merit:

Aperture array receivers form a key part of current and future SKA instrumentation. The SKA Mid-Frequency Aperture Array (MFAA) will make use of aperture array antennas in the 500 – 1500 MHz range. Each of these antennas would need a low noise, but uncooled receiver, which may consist of a low-noise amplifier (LNA), true time delay (TTD) network for analogue beamforming at a tile level, and an analogue-to-digital converter (ADC). Monolithic integrated circuit (IC) integration of such a receiver would allow for low-cost mass-production, but co-integration of separate dies in a suitable package may also be advantageous.

The integration (either monolithic or co-packaged) of the receiver poses a number of non-trivial problems, including the design of a broadband LNA with exceptionally low noise figure, mitigation of ADC switching noise leaking into the LNA input port, calibration and stability of the broadband TTD, and low power consumption to simply thermal management of the receiver station.

With the viability of potentially low-noise current-mode digitizers already evaluated and dismissed for excessive power consumption, attention should now be turned to noise shielding, exploring new concepts in the rapidly developing field of microelectronic EMC studies. For noise leakage in monolithic CMOS, grounded deep-trench isolation has been found to offer the best suppression of conducted RFI in the bulk substrate, electromagnetic bandgap structures for propagating surface waves in the oxide back-end, and conventional filtering for conducted noise suppression on power rails. What has not yet been established, however, is the proportional contribution of these mechanisms to the effective increase in noise figure, and whether the improved performance justifies the increased die area cost of suppressing passive networks. The potential benefit of silicon-on-insulator (SOI) integration, where the device channels are dielectrically isolated, also still needs to be investigated, as well as the role packaging of the die plays.

In the case of multi-chip co-packaged integration, there is a plethora of rapidly developing packaging technologies to consider (3D stacking, FCCSP, eWLB, to name a few) for this rather unique application. While substrate noise coupling may be addressed in this way, the effect of interconnect loss and interconnect variability are significant risks to be mitigated; optimal partitioning of constituent chiplets (especially given the option of heterogeneous semiconductor use) should therefore be seen as an active research question, as well as the functional use of interconnects as circuit design elements.

As for LNA design techniques, it has been found that sub-0.2 dB NF is feasible in this frequency range with modestly scaled CMOS nodes, but the achievable performance of more advanced nodes (as well as SOI and SiGe BiCMOS) remains unknown. In addition, the design techniques used to implement these LNAs still make extensive use of conventional inductors (which result in higher resistance and, subsequently, higher thermal noise contribution at the input) for gate / base matching, which may be mitigated significantly with more advanced differential and neutralization techniques. In addition, more advanced nodes may offer the option of acceptable performance with lower power consumption, exploiting e.g. the Gm/ID design technique for biasing in a weaker inversion regime.

As for the TTD, it may be possible to compensate for process and environmental variation with indirect measurement, as opposed to explicitly measuring the TTD by switching it from the circuit. These techniques have been demonstrated (to some extent) for phase shifters, but not in this medium nor over this bandwidth.

It is not envisaged that this study will explore all of these research areas exhaustively, but that the most important barriers to single-package AA receiver deployment will be identified and addressed in a manner that brings the state-of-the-art closer to a viable production model of the receiver.

2. Feasibility:

The M4 lab at the University of Pretoria has significant experience in RF CMOS design, including prior work on single-IC integrated MFAA receiver. The lab is further equipped with all the necessary laboratory facilities for measurement (including wafer-probed microelectronic measurements and basic packaging equipment), as well as software for circuit and system modelling. Funding to support semiconductor prototyping is also in place, along with access to various suitable foundries and processes.

Potential objectives for this project would be:

Y1: Literature review. Study of noise coupling modes and design of mitigation techniques. High-level integration study. First round LNA and ADC designs. First prototyping round.

Y2: Evaluation of first prototyping round; specifically of noise mitigation. Design of TTD circuit. Design of TTD calibration circuit. Implementation of flatness control measures. TTD prototyping and characterization.

Y3: Full integration of LNA-TTD-ADC chain. Global optimization for noise, stability and power consumption. Final prototyping and characterization round.

3. The project relates to “Radio astronomy antennas and receiver systems”. SKA SA is a member of the MFAA consortium, and the development of a single-chip / single-package receiver would be an important contribution to its work.

4. The preferred candidate would have completed a Master’s degree in RF circuit design, with a firm background in electromagnetics as well.