Details of Research Project

Section A: Overview of the Research Project

1. Calibration of wideband interleaved ADC structures
2. Engineering
3. Masters

4. Abstract of research project
Reliable, wideband signal digitization is critical to the development of SKA Band 5 (4.8-15.3 GHz) observations. The current baseline design employs a single, 4-bit, 16 Gsps monolithic flash ADC. Due to its limited effective number of bits (ENOB) at these high frequencies and wide bandwidth, an alternative digitization strategy is considered. It will require multiple interleaved digitizers, with accurate and stable time delays and gain calibration. This project will aim to develop improved digitizer time synchronization and gain calibration techniques. Digital signal processing (DSP) techniques will be developed to optimize the delay of multiple digitizer cores inside an ADC module, while RF techniques (to optimize delay between two separate ADC modules) will be pursued as a secondary goal.

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Section B: Details of Research Project

1. Scientific/Engineering merit:

SKA Band 5 (4.8-15.3 GHz) will require digitizer (or analog-to-digital converters, ADCs) that challenge the state-of-the-art in digitization speeds with commercially available ADCs. Typically, to reach the required sampling rates, multiple ADCs are interleaved. Time-interleaved analogue to digital converters (TI-ADC) are widely used in high speed data communication systems, instrumentation and measurement systems. They have risen in popularity as they alleviate problems like limited comparator regeneration time, amplifier settling time and amplifier linearity issues related to power consumption, all of which are associated with achieving high sampling rates using other architectures. This is achieved by using multiple sub-ADCs in parallel, each one slightly offset relative to the others in the time domain. The technique may also be applied to parallel placement of multiple ADC modules on the same PCB.

The bulk of the commercial and academic developments of both discrete PCB based system level and RF system-on-chip (SoC) TI-ADC families are largely driven by the increasing demand in wide-band communication systems. This limits the available experimental data

from the manufacturer to limited frequency bands, rather than the entire bandwidth. For wide-band radio astronomy applications, it is essential to have performance evaluation over the entire bandwidth of the TI-ADC. This warrants further investigation into the wideband performance of the proposed hardware architecture.

Second, and even more relevant to the above, the dynamic performance of a TI-ADC system is significantly deteriorated by channel mismatches due to component mismatches among the distinct analogue sub-ADCs, or even ADC cores inside a multi-core packaged ADC. The sampled signal in each sub-ADC suffers from gain and offset mismatches, as well as timing skew. This is compounded by the variation of these over frequency in wideband setups. Finally, interleaving spurs also introduce unwanted spectral components.

TI-ADC systems will, therefore, greatly benefit from a calibration strategy aimed specifically at transforming them into wideband ADCs. However, which practically realisable FPGA based strategy is best suited to address the needs of a radio astronomy receiver remains an unanswered question in literature. In addition, wideband high-frequency layout and control techniques for interleaving multiple ADC modules similarly remains an open question.

2. Feasibility:

A recent study (Dec 2021) by Oxford researchers have evaluated an RFSoC based TI-ADC using floating point, off-line post-processing, to isolate the performance of the ADCs from any concerns about fixed-point arithmetic in the FPGA,as well as a single-channel spectrometer implemented in the FPGA operating in real-time. This was done without the proposed calibration in this proposal.

A number of calibration methods are known, which may feasibly be pursued toward a viable calibration strategy. They can be broadly divided into two categories, being i) analogue and mixed signal techniques, and ii) all digital techniques. The most popular digital approaches include non-blind and blind techniques, with the latter being the focus of this project. The application of any of these, or in combination, could lead to a feasible and synthesizable FPGA based solution, although this has not yet been demonstrated.

The Carl and Emily Fuchs Institute for Microelectronics at the University of Pretoria has significant experience in the design of RF and microwave components, as well as digital signal processing techniques. The lab is further equipped with all the necessary laboratory facilities for measurement, as well as software for circuit, EM, and system modelling and digital design. A suitable TI-ADC based sampling analogue and mixed signal front-end, as well as suitable FPGA based processing platform with sufficient RF bandwidth processing capability and resources, are also available.

The potentially expected intermediate milestones and associated timeframes towards attaining the overall objectives of the project would include:

Y1: Literature review. Digital simulation of the calibration methodology in a high level language. Design and verification of experimental setup.
Y2: VHDL/FPGA design, implementation, prototyping and testing. Experimental measurement and performance characterisation.

3. SARAO research priority areas

The project directly ties in with the following main SARAO postgraduate research focus areas in 2022:

> *5.2.1 Radio astronomy antennas and receiver systems (including digitisation) associated with supported and hosted instruments.*
>
> *5.2.2 Real-time digital signal processing instrumentation for radio astronomy, specifically using FPGA and GPU platforms.*

The proposed techniques, if successful, will lead to increased bandwidth performance and improved measurement accuracy of currently installed and operating SARAO receivers. It will also develop critical skills in digital signal processing for radio astronomy.

4. *The preferred candidate* would have at least a firm undergraduate background in digital system and algorithmic design in VHDL/FPGA.